APPLICATION NOTE

Large Signal Output Optimization for Kodak High-Gain Interline CCDs

August 23, 2004
Revision 1.0

General description

This application note applies to the following Kodak Interline Image Sensors and should be used with each device's specification sheet:

- KAI-2020 Interline CCD
- KAI-4021 Interline CCD

Although the KAI-0340 interline CCD has a 30 μV/e- charge to voltage factor similar to that of the KAI-2020 and KAI-4021, the recommendations in this application note do not apply to that sensor because the reset drain and the output gate voltages are biased on the sensor and can't be adjusted by the user.

This application note explains and summarizes the voltage adjustments needed and trade-offs to be considered when designing to achieve maximum charge capacity with the KAI-2020 and KAI-4021 Interline CCDs.

Due to the high sensitivity (30uV/e-) of the CCD, the output amplifier is slew rate limited for large signals when operating at high pixel frequencies. For example, the amplifier can't swing to 1200mV or 40ke- output signal at 40MHz.

Depending on the pixel frequency and charge capacity desired, some voltage adjustments may be recommended for optimized performance. This is summarized in the tables below:

Pixel Freq.	Reset Clock (V)		Output Gate	Reset Drain	Saturation	Saturation	Dynamic
(MHz)	Low	High	(V)	(V)	Signal (mV)	Signal (ke-)	Range (dB)
40	-3	2	-2.0	12.0	600	20	60
20	-3	2	-2.0	12.0	600	20	62
20	-3	2	-2.0	12.0	1200	40	68
20	-3	4	-3.0	13.0	2400	80[1]	74

Notes:
1. 80,000 electrons achievable in summed interlaced or binning modes.

Table 1. Voltage Summary for KAI-4021 CCD

Pixel Freq.	Reset Clock (V)		Output Gate	Reset Drain	Saturation	Saturation	Dynamic
(MHz)	Low	High	(V)	(V)	Signal (mV)	Signal (ke-)	Range (dB)
40	-3.5	1.5	-2.0	12.0	600	20	60
20	-3.5	1.5	-2.0	12.0	600	20	62
20	-3.5	1.5	-2.0	12.0	1200	40	68
20	-3.5	3.5	-3.0	13.0	2400	80[1]	74

Notes:
1. 80,000 electrons achievable in summed interlaced or binning modes.

Table 2. Voltage Summary for KAI-2020 CCD

For high signal levels, it is strongly recommended to set Output Gate and Reset Low at the same voltage level or less than 0.5V apart. This helps prevent charge from spilling out of the floating diffusion.
Setting the Reset Drain at the higher voltage of 13 Volts increases the charge capacity of the floating diffusion. Increasing the Reset High voltage level improves the capability to fully reset the floating diffusion. This ensures that charge is not left behind on the floating diffusion even when the signal level is very high.

Output Architecture

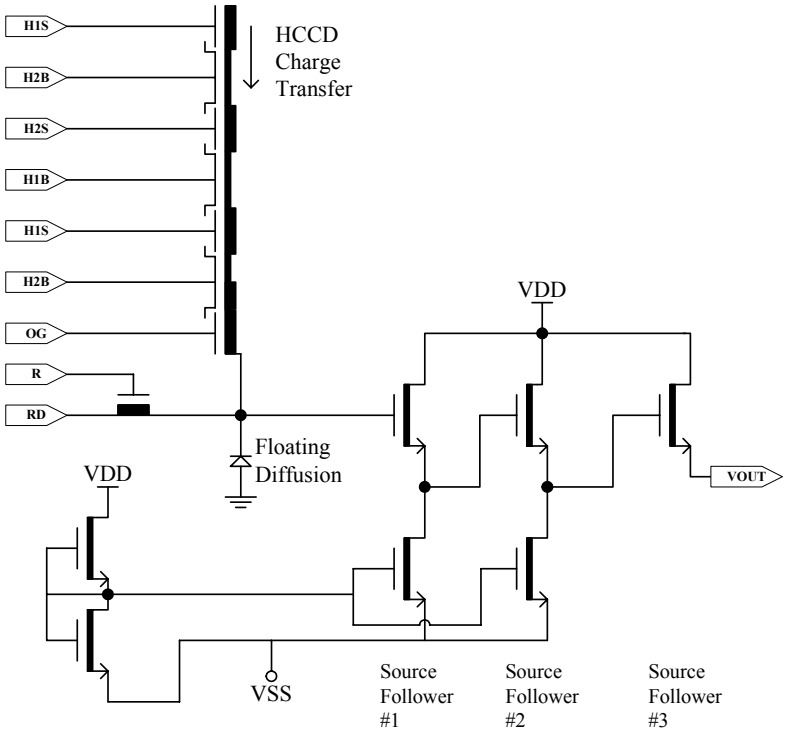

Figure 1 - Output Architecture

Charge packets contained in the horizontal register are dumped pixel by pixel onto the floating diffusion (fd) output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential charge is determined by the expression $\Delta Vfd=\Delta Q/Cfd$. A three-stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain. The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of microvolts per electron ($\mu V/e^-$). After the signal has been sampled off chip, the reset clock (R) removes the charge from the floating diffusion and resets its potential to the reset drain voltage (RD).

When the image sensor is operated in the binned or summed interlaced modes there will be more than 20,000 electrons in the output signal. The image sensor is designed with a 30µV/e charge to voltage conversion on the output. This means a full signal of 20,000 electrons will produce a 600mV change on the output amplifier. The output amplifier was designed to handle an output swing of 600mV at a pixel rate of 40MHz. If 40,000 electron charge packets are generated in the binned or summed interlaced modes then the output amplifier output will have to swing 1200mV. The output amplifier does not have

enough bandwidth (slew rate) to handle 1200mV at 40MHz. Hence, the pixel rate will have to be reduced to 20 MHz if the full dynamic range of 40,000 electrons is desired.

The charge handling capacity of the output amplifier is also set by the reset clock voltage levels. The reset clock driver circuit is very simple if an amplitude of 5V is used. If you only want a maximum signal of 20,000 electrons in binned or summed interlaced modes, then a 40MHz pixel rate with a 5V reset clock may be used. The output of the amplifier will be unpredictable above 20,000 electrons so be sure to set the maximum input signal level of your analog to digital converter to the equivalent of 20,000 electrons (600mV).

Performance Data - Linearity

40,000 electrons at 20MHz

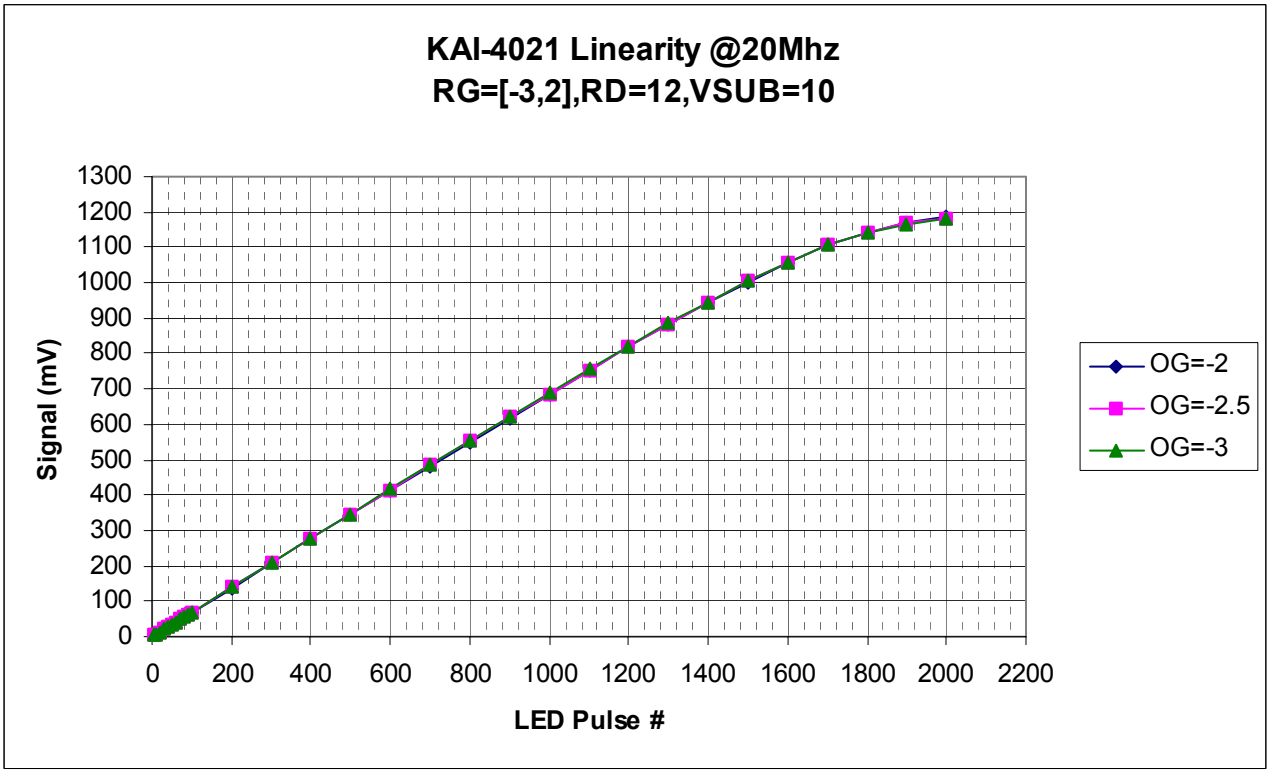

Figure 2 – Linearity Plot

80,000 electrons at 20MHz by 2x2 binning mode

The following are example plots from the KAI-4021 Interline CCD to illustrate the linearity performance from low signal level to high signal levels equivalent to 80k electrons:

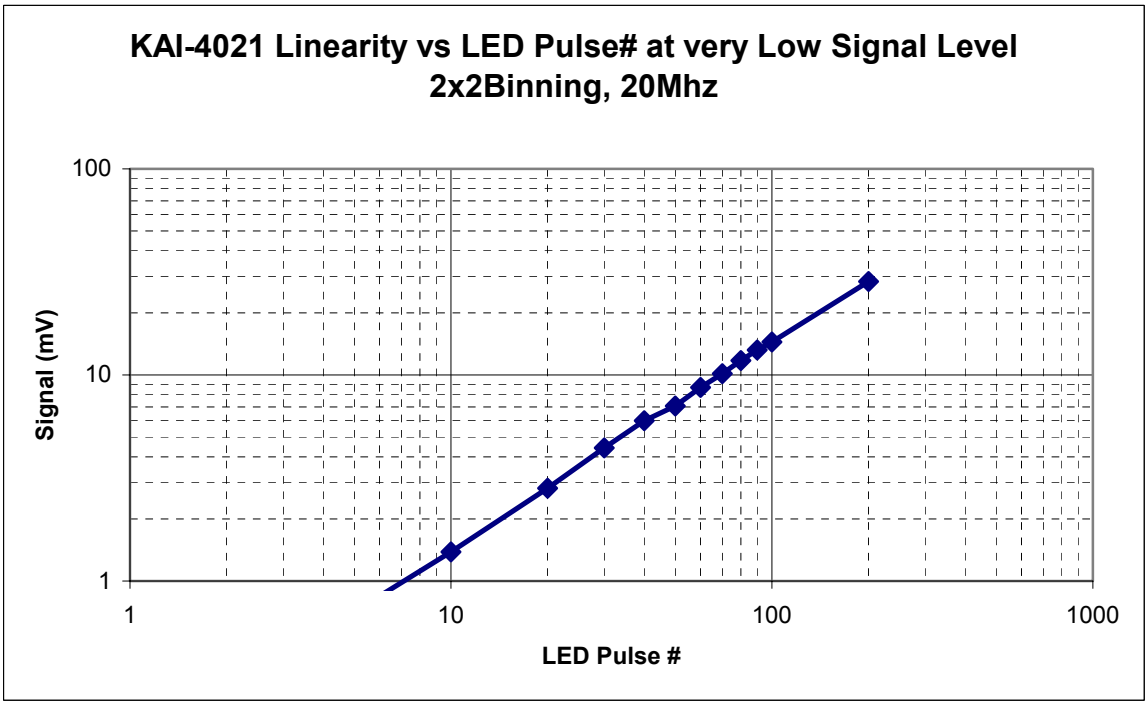

Figure 3 – Linearity at low signal level

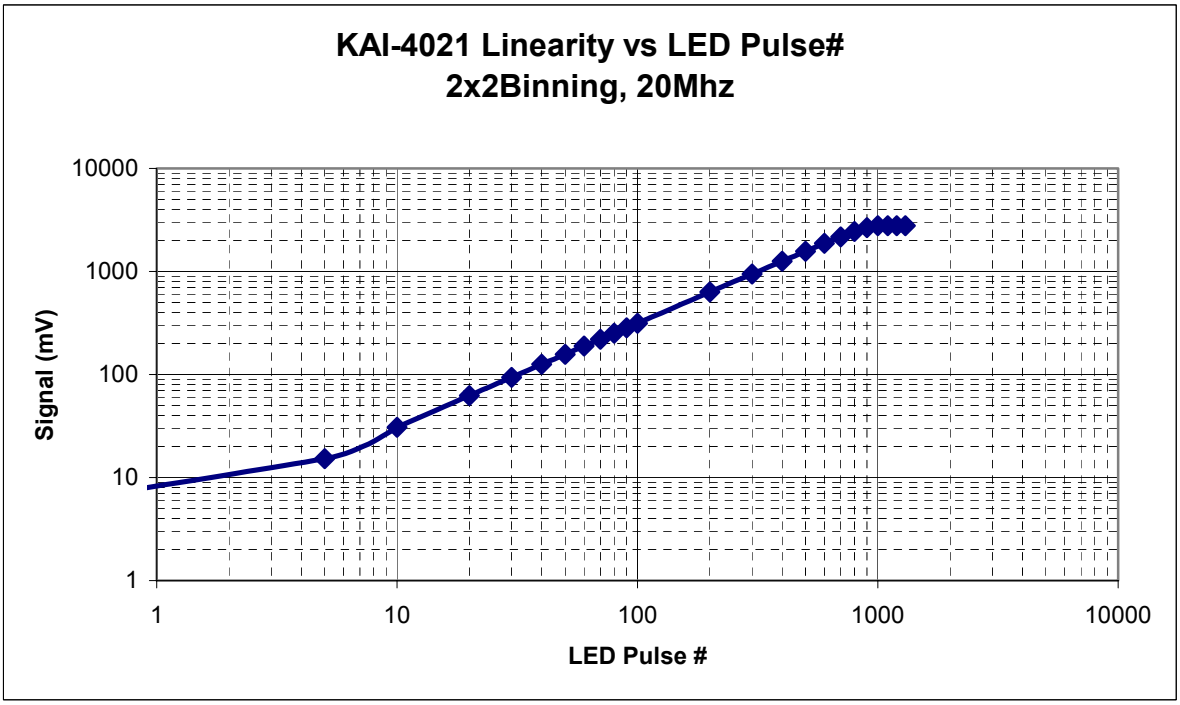

Figure 4 – Linearity across full signal level

The Photo Response Non-Linearity (PRNL %) plot describes by how much the measured signal output deviates from the ideal fit line.

The fit line uses two data points from Figure 2 for the PRNL calculation:

- The zero referenced data point at the low end representing no signal output, the dark reference is subtracted from all the data point values
- The data point that represents 80,000 electrons of signal

Then the measured CCD output signal is compared with the calculated fit signal to obtain the percent (%) non-linearity.

The values obtained can easily vary depending on how the user selects the upper data point. Therefore it is important to note how a particular test was performed for meaningful interpretation.

The example performance data demonstrates that both the KAI-4021 CCD and KAI-2020 CCD have excellent linearity over a wide range of signal levels.

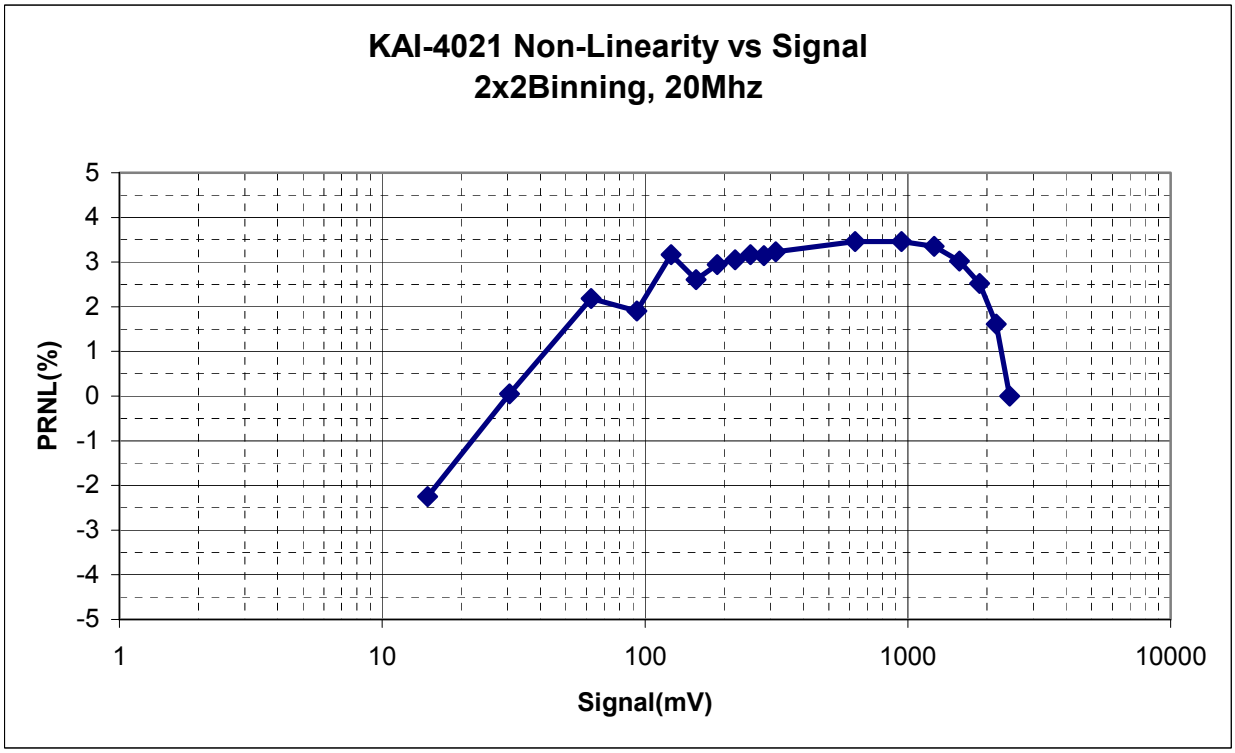

Figure 5 – Photo Response Non-Linearity (PRNL%)